REMARKS

Reconsideration of the instant application is respectfully requested. The present amendment is responsive to the Office Action of August 19, 2003, in which claims 1-20 are presently pending. Claims 15-20 have been withdrawn from consideration as being drawn to a non-elected invention. Of the remaining pending claims, claims 1-5 and 8-12 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 6,072,233 to Corisis, et al. In addition, claims 7 and 14 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Corsis, et al. However, the Examiner has further indicated that claims 6 and 13 are allowable over the references of record. For the following reasons, it is respectfully submitted that the application is in condition for allowance.

As an initial matter, the title of the invention has been amended to read -- JOGGING STRUCTURE FOR WIRING TRANSLATION BETWEEN GRIDS WITH NON-INTEGRAL PITCH RATIOS IN CHIP CARRIER MODULES --, thus addressing the Examiner's requirement on page 2 of the present office action.

With regard to the rejections based on the art of record, claims 1 and 8 have been amended to more particularly point out that the first and second translation layers are further configured so as to fan out the signals from the first grid to the second grid. Support for this claim feature is found at least at page 4, line 13, and in Figure 4. This feature, however, is not taught or suggested by Corisis. Rather, Corisis teaches a grid array package "that allows the stacking of one array upon another." (col. 2, lines 36-38) Moreover, as stated in column 2, lines 61-65, Corisis teaches that "[t]his isolated connection connects to an adjacent ball on a different FBGA stack above or below the particular isolated connection since in ***common pin layouts of the devices stacked together***, each device requires an isolated connection to the PC board." (Emphasis added)

In other words, the conductor patterns are configured not to fan out connections between layers, but to allow stacking of like-configured substrates. As such, Corisis does not teach the claimed jogging structure having first and second translation layers (as set forth above) wherein the translation layers are further configured to fan out the signals. Accordingly, each of the §102 and §103 rejections has been overcome, and it is respectfully requested that the same be withdrawn.

Finally, claim 5 has been amended, as indicated above, to address the Examiner's objection thereto, and it is respectfully requested that the same be withdrawn.

For the above stated reasons, it is respectfully submitted that the present application is now in condition for allowance. No new matter has been entered and no additional fees are believed to be required. However, if any fees are due with respect to this Amendment, please charge them to Deposit Account No. 06-1130 maintained by Applicants' attorneys.

Respectfully submitted,
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